

A Low Power and Efficiency Pipelined FFT Processor for OFDM Communication System

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ABSTRACT

This paper comprises of an investigation of Fast Fourier Transform (FFT) designs which are the foundation of any OFDM based remote organizations. By utilizing the FFT ideas we are in fact in building up an effective structures for remote organizations which are normal in all over. This paper will explicitly address the force proficient plan of a FFT processor as it identifies with arising OFDM correspondences, for example, intellectual radio. Increasing paces and unpredictability of remote correspondence frameworks have required the advancement and progression of superior sign handling components, Our ideas are simply founded on being developed we need by utilizing (FPGA), These assets incorporate force, memory, and chip region. Progressing research looks to enhance asset utilization just as execution. Configuration turns into an equilibrium and bargain of adaptability, execution, multifaceted nature, and cost.

Keywords: FFT, OFDM, FPGA.

1. INTRODUCTION

Cognitive radio is a strategy for remote correspondence via powerfully adjusting the various subcarriers to transmission changing conditions in the correspondence channels. The subcarriers are empowered by a balance plot referred to as orthogonal frequency division multiplexing (OFDM). OFDM changes over a high information rate signal into various lower information rate signals for concurrent transmission through various channels. The Fast Fourier Transform processor is the core of OFDM that empowers its quick and productive adjustment of signs. The FFT calculation is a quick calculation of the Discrete Fourier Transform which is a fundamental part of the balance plot utilized in OFDM. As the FFT processor is the most computationally escalated segment in OFDM correspondence, an improvement in the force productivity of this segment can impactly affect the general framework. These effects are huge considering the quantity of portable and far off specialized gadgets that depend on restricted battery-fueled activity. This undertaking will fill in as an investigation of current FFT processor calculations and models just as improvement methods that mean to decrease the force utilization of these gadgets. Super Wideband (UWB) Technology brings the accommodation and portability of remote correspondences to rapid interconnects in gadgets all through the computerized home and office. Instead of wired connection, this technology enables wireless connection for transmitting video, audio, and other data with high data speed and low power consumption. After IEEE 802.15.3a was withdrawn in the Spring of 2006, Multiband-OFDM has been controlled by ECMA International. However, some key issues need to be solved for designing CMOS based Multiband-OFDM UWB solution in support of the low power requirement. One of the issues focuses on its FFT (Fast Fourier Transform) block, which takes 25% design complexity of the total digital baseband transceiver [1]. Although many results have already been published in this research area in the past few years [4], some key problems still exist and need to be improved for the speed, area and power consumption consideration. In light of ECMA-368, for the necessity of Multiband-OFDM framework, this FFT processor should deal with a couple hundred MHz, which makes it hard to execute. Furthermore, since this framework focuses for the remote convenient gadgets, little territory and low force utilization are likewise basic. Hence, this theory centers around the region and force utilization improvement under the ECMA-368 standard necessities. To achieve this goal, a couple of stages should be followed. The underlying advance is to find the points of interest for this FFT processor, which is directed by the Multiband OFDM UWB standard. The movement requires the examination on OFDM and UWB development and the goals of its FFT processor. Resulting to describing the points of interest, overhauled FFT count and configuration should be used for these subtleties. There are an enormous number of FFT calculations and structures in the sign preparing writing [7]. Subsequently, the condition of workmanship calculations and structures should be broke down and analyzed. In view of various calculations and designs, diverse force utilizations, zone and speed of the processor will be accomplished. So their ASIC appropriateness should be examined and the exertion should be

centered around the picking calculations and structures and improvement. Besides, the improvement space should be investigated and the engineering should be additionally upgraded. The proposed calculation and design should be approved by reenactment before usage. After that, this circuit needs to be implemented with VHDL. The synthesis step is followed by using both Simplify Pro targeted for FPGA and style Compiler for ASIC. For this, each carrier may use one among the several available digital modulation techniques.

2. LITERATURE SURVEY

FFT pruning calculations and structures [9] are intended for figuring specific recurrence receptacles on the range however not for mirroring the asset designation conspire in the OFDMA framework. Subsequently in this concise, we propose the unfinished stored FFT calculation for common asset block (RB) dispersions within the OFDMA framework. Besides, we design a mixed pipelined/cached-FFT processor with constellation and power awareness. Finally, we implement and measure the FFT processor chip to point out its energy efficiency.

2.1. PARTIAL CACHED – FFT ALGORITHM FOR Resource Block ALLOCATION:

By and large, considering the genuine equipment plan, the exactness of FFT/IFFT module is a significant plan factor of framework execution. By and by, fixed-point number juggling is utilized to actualize FFT calculations in equipment since it is beyond the realm of imagination to expect to keep limitless goal of coefficients and activities. All coefficients and information signals must be spoken to with number of pieces in paired configuration relying upon the tradeoff between the equipment cost (memory use) and the precision of yield signals. As a rule, every increase may acquaint a mistake due with adjusting tasks or truncations, which is alluded as number juggling quantization blunder. The theoretical performance evaluation has been given in previous works. Several previous works have analyzed the effect of fixed-point arithmetic for radix-2 FFT. In this section, we derive the equivalent matrix form of both DIF and DIT FFT algorithms. Although the alternative DIT and DIF FFT algorithms have the same multiplicative complexity, sequence of butterfly stages and twiddle factor stages is re-versed. In other words, the signal flow of two alternative representations is actually the mutual mirroring of each other.

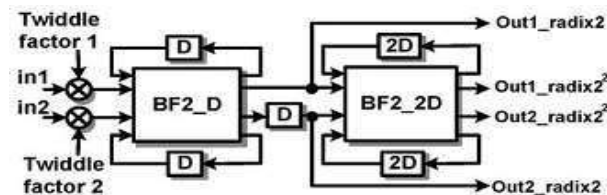


Fig-1 FFT ALGORITHM FOR Resource Block ALLOCATION

2D pipelined. The proposed 64 to 1024-point cached-FFT processor, as shown in Fig. 1, consists of a radix-2/22 pipelined butterfly processor, cache sets, and main memory. We propose a dual-delay feedback (DDF) butterfly architecture, to avoid the idling of the butterfly unit (BU) the traditional single-delay-feedback architecture. Two radix-2 sequences share the butterfly units by using a delay register the first butterfly. The time schedule for the dual-stream processing. The gray and slash blocks of time slots represent the operations of BF2_D and BF2_2D butterfly units, respectively. Thus, the butterfly processor can achieve 100% utilization rate. If the radix-23 butterfly processor is used for the dual streams, the latency will be increased, because more delay registers must be inserted for 100% utilization. If radix-4 and four streams are used, the cost will significantly grow. Therefore, the radix-2/22 dual-stream architecture is a compromise of the cost and the throughput.

2.2. CACHE/MEMORY ARCHITECTURE:

We use two cache sets to facilitate the data transfers between butterfly processor and the cache sets and between the cache sets and the main memory. The cache sets must perform two write operations and two read operations in one clock cycle for the dual-stream processing. To avoid the utilization of the four-port cache and simplify the control complexity, we divide each cache set into two banks for even and odd addresses.

The odd/even address detector serves to detect whether the data is accessed in the correct bank and to exchange the access positions if necessary. Thereby, we can carefully manipulate the computational time schedule to ensure that one even address and one odd address are write operations in one cycle. Therefore, we divide the main memory into two banks of single-port 512-word static random-access memory (SRAM) for even and odd memory addresses.

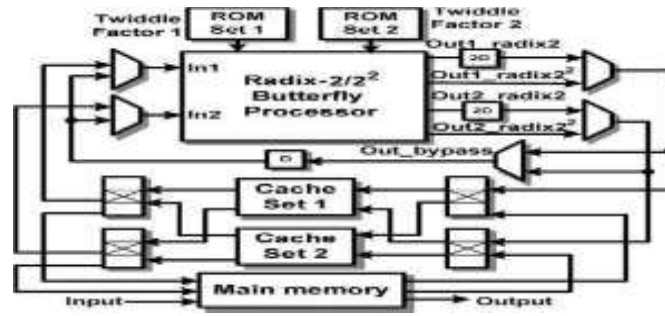


Fig-2 CACHE/MEMORY ARCHITECTURE

3. EXISTING SYSTEM

The input file stream is split into N parallel low band- width modulated data streams. thanks to orthogonality of subcarriers they are doing not interfere with each other . Each subcarrier features a low symbol rate .But the mixture of subcarriers carrying the knowledge in parallel allows for top data rates. Low image rate is utilized to decrease the matter of Inter Symbol Interference (ISI)8-10. Before regulation the transmitter phase of an OFDM handset takes information, Converts the information and encodes it into a sequential stream. The age of OFDM signal is happens by utilizing Inverse Fast Fourier Transform (IFFT). Switch measure happens in recipient stage.

3.1 Transmitter

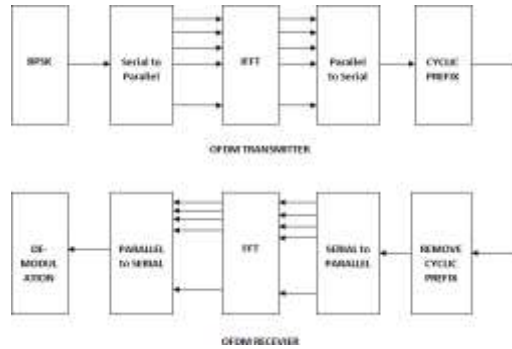


Fig.3 Block diagram of OFDM Transmitter and receiver.

3.1.1 BPSK Modulation

The BPSK Modulation scheme is one of the Phase shift keying technique which can be used for the modulation with 180 deg phase shift keying is applied.

3.1.2 Serial to Parallel

The Serial to parallel block contains Technique that converts serial form input data to parallel form outputs, it converts the data serial inputs to parallel outputs that can be works after getting all inputs in the parallel signal.

3.1.3 IFFT Block

The IFFT Block is converts the Input data from Frequency domain to Time domain outputs.

3.1.4 Cyclic Prefix

The Cyclic Prefix is block that assigns empty memory space with your input data in the base of 1/N value of the input is to be assigned for cyclic prefix memory.

3.1.5 Receiver Block

The Receiver block contains Remove cyclic prefix block, serial to parallel block, FFT Block, Parallel to serial block, Demodulation.

3.1.6 Remove Cyclic Prefix

The Remove cyclic prefix is removes the empty space that created in the transmitter block. The cyclic prefix. Memory is contains noise and errors that can be removed in this block.

3.1.7 Fast Fourier Transform Block

The Fast Fourier Transform block is performs the input from time to frequency operations. The FFT blocks basically contains different type of radix based FFT architectures as follows,

- Radix-2
- Radix-4
- Mixed- Radix
- Split Radix

during this paper we propose the pipelined implementation of Radix-2 based single delay feedback (R2SDF), Radix-2 single delay commutator (R2SDC), combined architecture is implemented within the receiver architecture of OFDM

4. COMPUTATION TIME SCHEDULE:

Since the cache flush/refresh time is smaller than the one- ass processing time, the butterfly processor can continuously compute without an idle time slot. However, there are timing overlaps between the cache flushing/refreshing and part, appeared in Table 1.

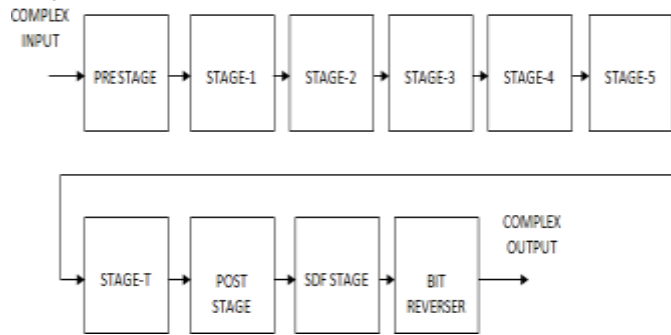


Fig.7 Proposed system block diagram.

The contrasting post-stage revamps back the new progression to the mind boggling setup. The SDC stage ($t = 1, 2, \dots, \log_2 N - 1$) contains a SDC PE, which may accomplish 100% math asset usage of both complex adders and sophisticated multipliers. Last, the even information are recovered in ordinary request. Along these lines, the touch reverser requires just $N/2$ information support. The last phase of Single Delay Feedback (SDF) is indistinguishable from the radix-2 Single Delay Feedback (SDF), containing a perplexing snake and a complex subtractor. By utilizing the altered tending to method12, the information with an even file are composed into memory in typical request, and they are then recovered from memory in bit turned around request while the ones with an odd file are reversed order.

Normally the Fast Fourier Transform architectures are working based upon the parallel architectures, so FFT's are consume large area and latency, in order to perform low area and latency we are in deed in develop- ing the pruning the FFT's with help of Pipelining Data path, feed forward, feed backward. And some various architectures for reducing the area and delay of the FFT processors, there are various radix-2 based architectures such as R2MDC, R2SDF, R2SDC; these architectures are very useful in making the pipelined operation of FFT's.

The proposed system consists of the architecture that can be have the stage-1, stage-2, stage-3, stage-4, stage-5 all are designed for 64-point FFT architectures, as shown in the Figure.

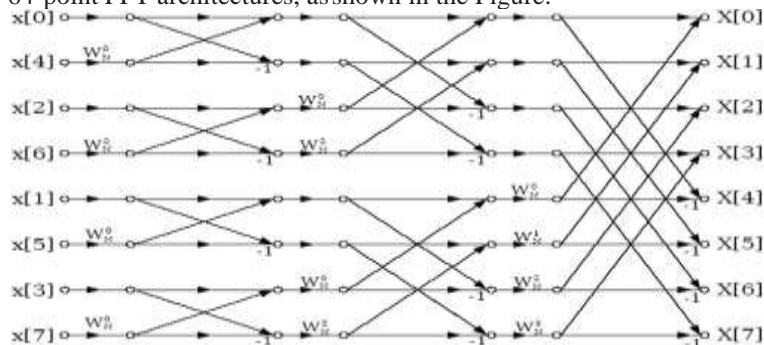


Fig.6 Block diagram showing pipelined based radix-2 FFT for 8-point

The proposed system consists of five stages and the stage-t which is also present in 64-point FFT architecture, All FFT based architectures are Operating based upon the parallel architectures, so we are proposing a Pipelined operation of FFT radix-2 architectures with combination of SDF-SDC architectures in order to achieve higher data rate. $\log_2(2N - 1)$ contains a SDC PE, which may accomplish 100% math asset usage of both complex adders and sophisticated multipliers four 8×13 caches, and four 128×13 ROMs. The function of the chip is verified, and its performance is measured using a digital test station. This chip can operate at maximum 51 MHz with 33.3 mw. We use the worst and best-case patterns for measuring the energy- saving capability of different RB allocation schemes, as shown in Fig. 4. Each curve represents a series of $\{1, 3/4, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64\}$ computed RBs in the whole OFDMA spectrum. We can see that the energy dissipation scales to the modulation order and the amount of the allocated resource

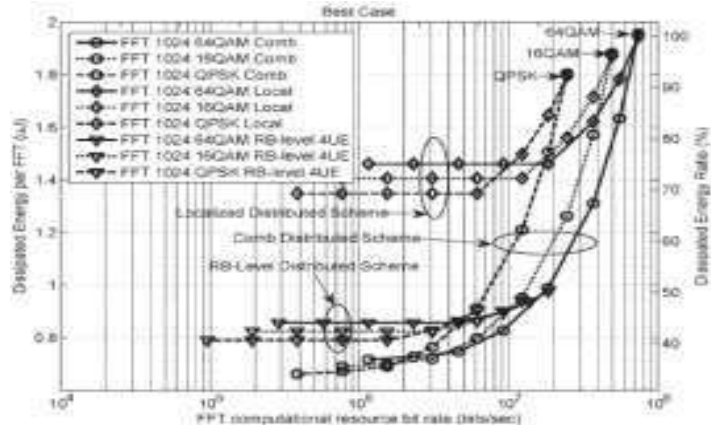


Fig.8 FFT radix

The comb-distributed scheme has the best performance, whereas the localized scheme has the worst performance. Note that the RB- level distributed scheme is a compromise between localized and comb-distributed schemes. Thus, its energy dissipation also lies between them. The energy scaling ranges from 1.90 to 0.64 nJ/FFT point for the 1024-point FFT, i.e., 67% energy can be saved in the FFT processor for minimal RB transmission. This result outperforms other cached- memory-based FFT chips. The latency for processing 1024-point full FFT is 61 μ s, which meets the 66.7- and 91.5- μ s OFDM symbol durations of the 3GPP-LTE and Mobile Wi MAX standards, respectively.

5. RESULT DUSSCUSSION

The output show in the figure

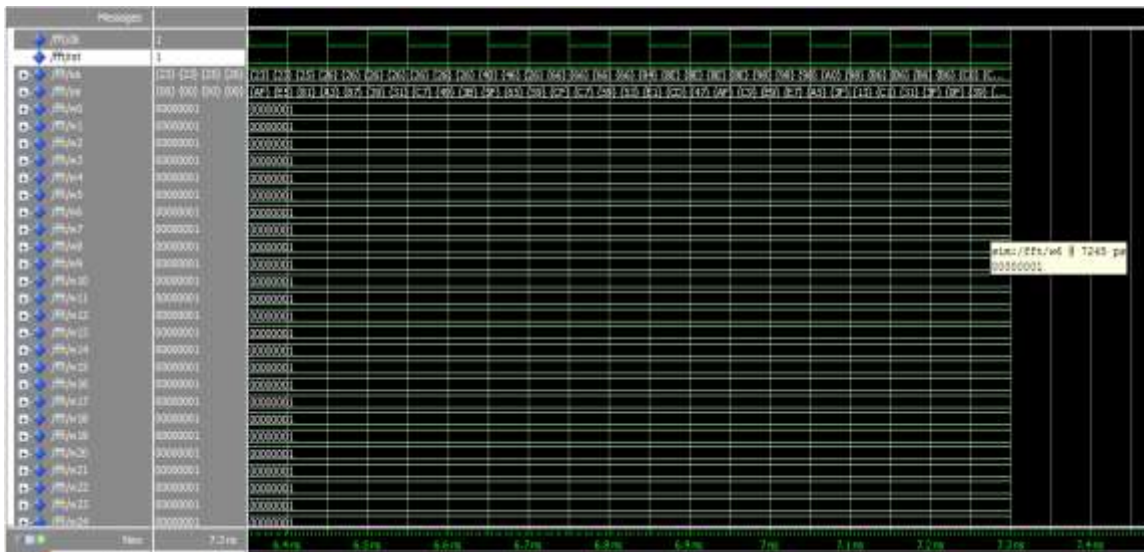


Fig.9 Output screen shot showing simulation waveform for Radix-2 based FFT.

Output screenshot showing simulation waveform for optimum multiplier based FFT.

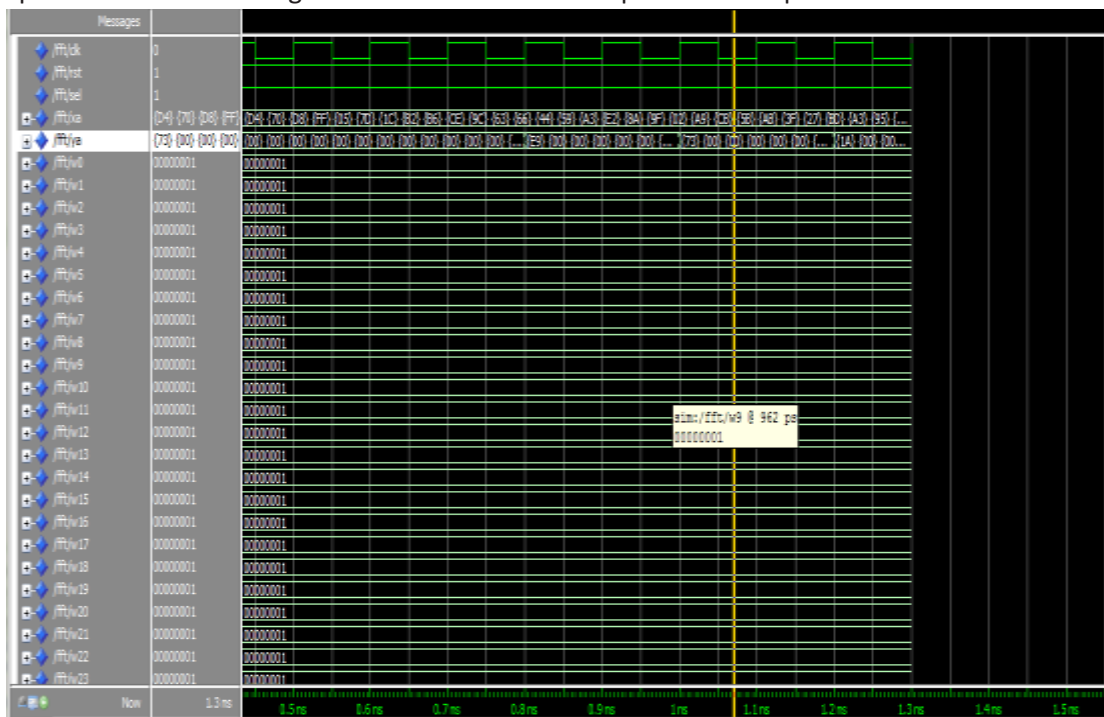


fig.10 Output screenshot showing the AREA (slices) and LUT for Radix-2 based FFT

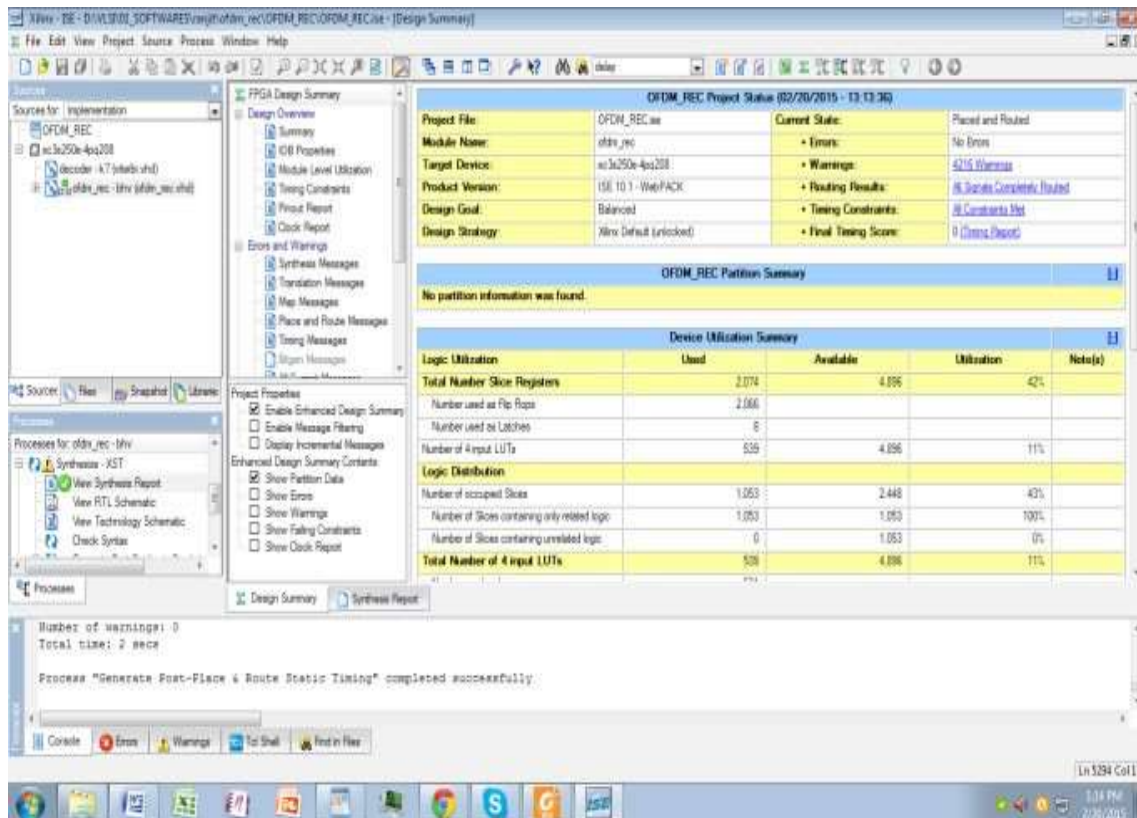


Fig.11 Output screenshot showing the AREA(slices) and LUT for radix-2 based FFT

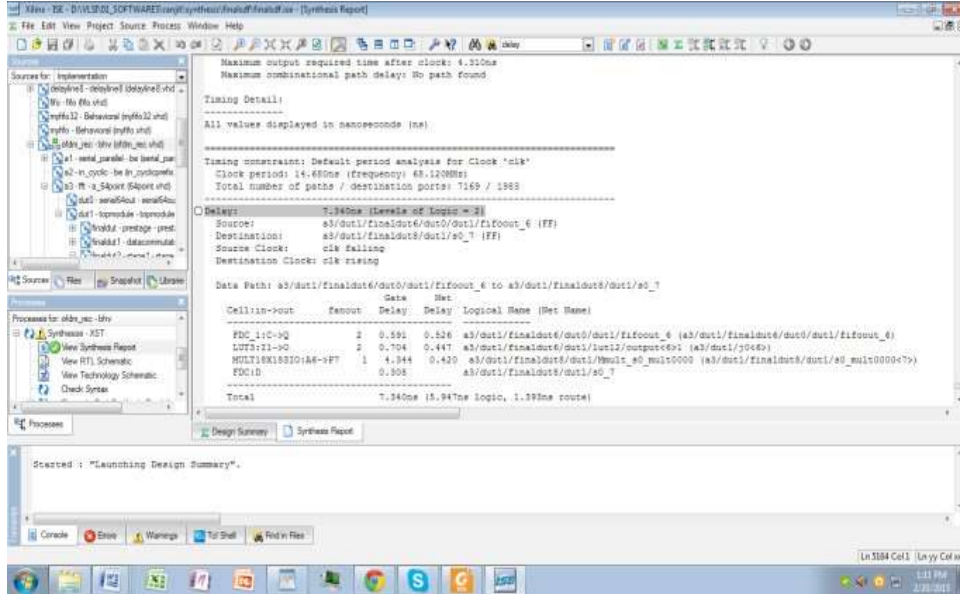


Fig.12 Output screenshot showing the FREQUENCY for Radix-2 based FFT.

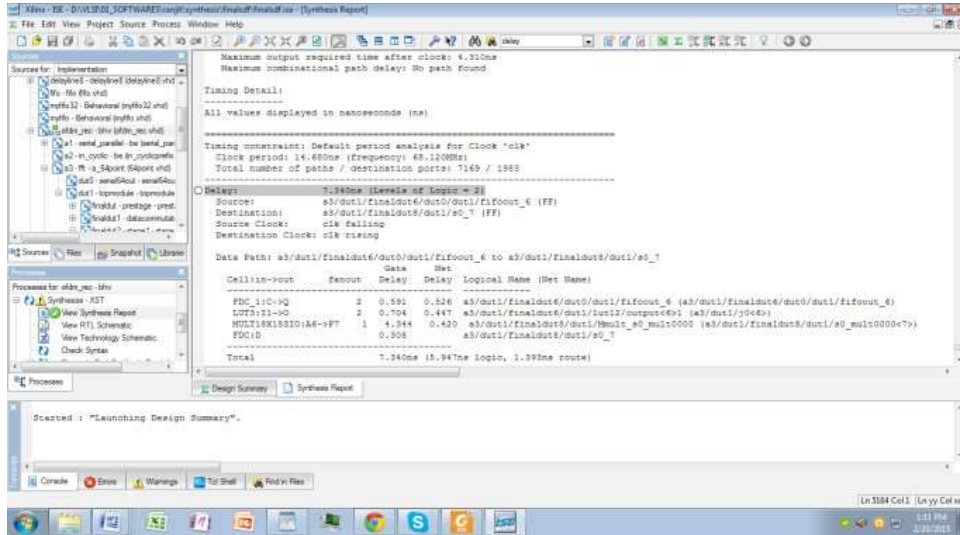


Fig.13 Output screenshot showing the AREA (slices) and LUT for optimum multiplier based FFT.

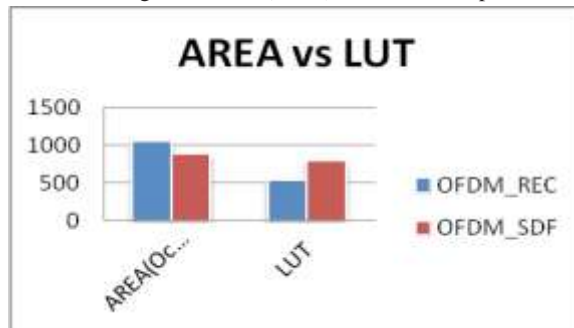


Fig.14 Comparison chart showing OFDM with Radix-2 based FFT with OFDM based optimum multiplier and their AREA (slices) and LUT

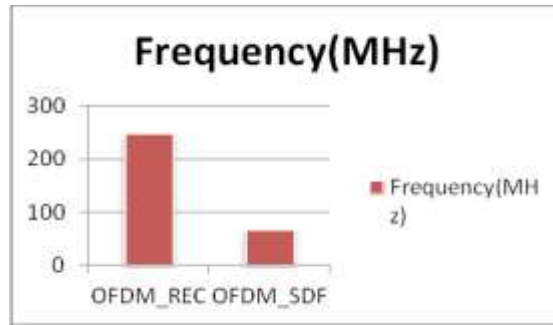


Fig15. Comparison chart showing OFDM with Radix-2 based FFT with OFDM based optimum multiplier and their Frequency

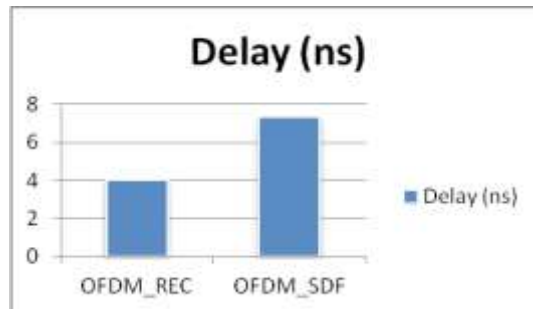


Fig.16 Comparison chart showing OFDM with Radix-2 based FFT with OFDM based optimum multiplier and their Delay.

Table 1. Comparison table showing OFDM Radix-2 based FFT with OFDM based optimum multiplier

	AREA (Occupied Slices)	LUT	Delay (ns)	Frequency (MHz)	Power (W)
OFDM_REC	1053	539	4.014 ns	248.128	2.772
OFDM_SDF	890	797	7.340 ns	68.120	0.295

The input file length of our proposed pipeline FFT processor may be a parameter which may be decided at the range of 128, 512, 1024 and 2048. Take 1024 points FFT as an example. At first, the 1024 points FFT is coded using MATLAB software. After the chosen FFT algorithm is valid, the architecture of the processor was modeled in VHDL language and functionally verified using Xilinx 12.3i software and timing simulation using ISIM SE software. During the timing simulation, a test bench file included the TEXTIO package was written to read input data and write FFT result. The behavioral simulation waveforms for the Processor are shown in figure 5

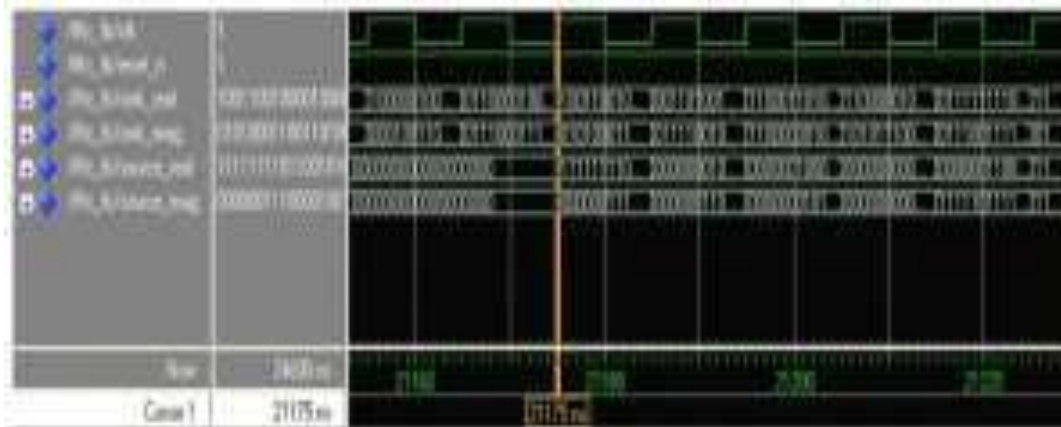


Fig.19 Simulation of 1024 point FFT

7. ACKNOWLEDGEMENTS

The creators might want to thank the mysterious commentators for their remarks which were useful in improving the quality and introduction of this paper. The results shows that the pipelined execution of this engineering is having low territory, high postponement and, less recurrence is removed from the outcomes, the deferral is high since the design is actualized pipeline structures.

8. REFERENCES

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